PIPO shift reg

//testbench

module shftregtb;

reg [3:0] d;

reg clk;

wire [3:0] q;

shftreg uut(.d(d), .clk(clk), .q(q));

initial begin

$dumpfile("shftreg.vcd");

$dumpvars(1);

clk=0;

forever #5 clk =~clk;

end

initial begin

d=0;

#100;

d = 4'b0011;

#100

$finish;

end

endmodule

//design

module shftreg(d, clk, q);

input [3:0] d;

input clk;

output reg [3:0] q;

always @(posedge clk) begin

q[3] <= d[3];

q[2] <= d[2];

q[1] <= d[1];

q[0] <= d[0];

end

endmodule